±15V Zero-Drift Operational Amplifier with Internal Capacitors

FEATURES

- High Voltage Operation: ±16V
- No External Components Required
- Maximum Offset Voltage: 10μV
- Maximum Offset Voltage Drift: 0.05μV/°C
- Low Noise 1.8μV_{P-P} (0.1Hz to 10Hz)
- Minimum Voltage Gain: 135dB
- Minimum PSRR: 120dB
- Minimum CMRR: 110dB
- Low Supply Current: 0.8mA
- Single Supply Operation: 4.75V to 32V
- Input Common Mode Range Includes Ground
- 200μA Supply Current with Pin 1 Grounded
- Typical Overload Recovery Time 20ms

APPLICATIONS

- Strain Gauge Amplifiers
- Electronic Scales
- Medical Instrumentation
- Thermocouple Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC®1150 is a high-voltage, high-performance zero-drift operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper amplifiers are integrated on-chip. Further, LTC's proprietary high-voltage CMOS structures allow the LTC1150 to operate at up to 32V total supply voltage.

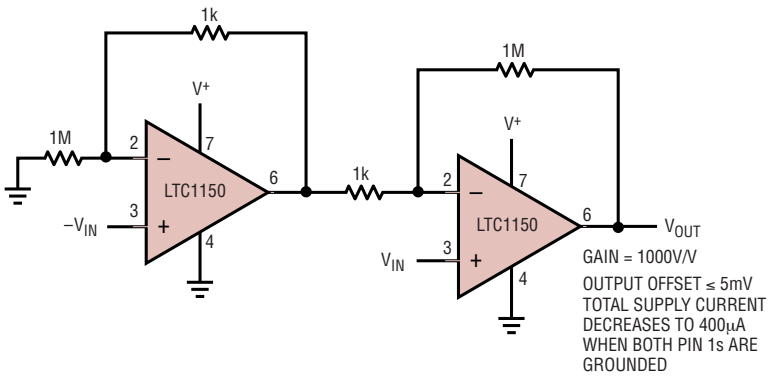
The LTC1150 has an offset voltage of 0.5μV, drift of 0.01μV/°C, 0.1Hz to 10Hz input noise voltage of 1.8μV_{P-P} and a typical voltage gain of 180dB. The slew rate of 3V/μs and a gain bandwidth product of 2.5MHz are achieved with 0.8mA of supply current. Overload recovery times from positive and negative saturation conditions are 3ms and 20ms, respectively.

For applications demanding low power consumption, Pin 1 can be used to program the supply current. Pin 5 is an optional AC-coupled clock input, useful for synchronization.

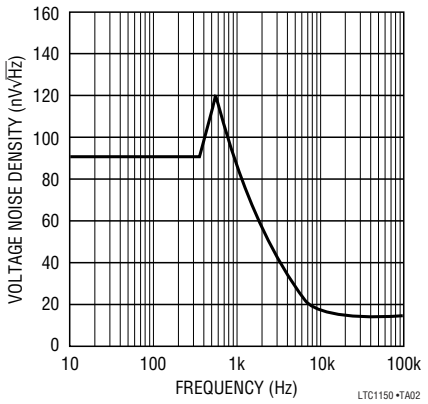
The LTC1150 is available in standard 8-lead, plastic dual-in-line package, as well as an 8-lead SO package. The LTC1150 can be a plug-in replacement for most standard bipolar op amps with significant improvement in DC performance.

TYPICAL APPLICATION

Single Supply Instrumentation Amplifier



Noise Spectrum

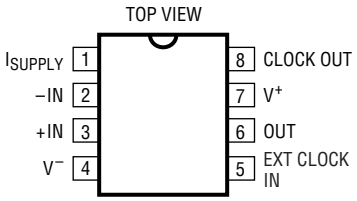


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 32V
Input Voltage (Note 2) ..... (V^+ 0.3V) to (V^- –0.3V)
Output Short Circuit Duration ..... Indefinite
Burn-In Voltage 32V

Operating Temperature Range
LTC1150M **(OBSOLETE)**.....–55°C to 125°C
LTC1150C ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



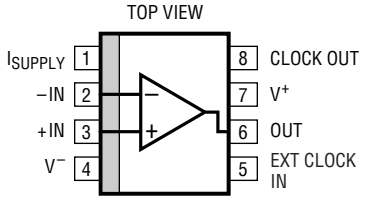
N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER: LTC1150CN8

J8 PACKAGE
8-LEAD CERDIP

OBSOLETE PACKAGE
Consider the N8 or S8 Package as an Alternate Source

ORDER PART NUMBER: LTC1150MJ8, LTC1150CJ8



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 110°C, θ_{JA} = 200°C/W

ORDER PART NUMBER: LTC1150CS8

S8 PART MARKING: 1150

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range otherwise specifications are at T_A = 25°C. V_S = ±15V, Pin 1 = Open, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1150M MIN	LTC1150M TYP	LTC1150M MAX	LTC1150C MIN	LTC1150C TYP	LTC1150C MAX	UNITS
Input Offset Voltage	(Note 3)			±0.5	±10		±0.5	±10	µV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
Long Term Offset Voltage Drift				50			50		nV/√mo
Input Offset Current		 ●		±20	±60 ±1.5		±20	±200 ±0.5	pA nA
Input Bias Current		 ●		±10	±50 ±2.5		±10	±100 ±1.0	pA nA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz, TC2			1.8			1.8		μV_{P-P}
	R_S = 100Ω, 0.1Hz to 1Hz, TC2			0.6			0.6		
Input Noise Current	f = 10Hz (Note 4)			1.8			1.8		fA/√Hz
Common Mode Rejection Ratio	V_{CM} = V^- to 12V	●	110	130		110	130		dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	120	145		120	145		dB
Large-Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±10V	●	135	180		135	180		dB
Maximum Output Voltage Swing	R_L = 10kΩ		±13.5	±14.5		±13.5	±14.5		V
	R_L = 10kΩ	●	10.5/ –13.5			10.5/ –13.5			
	R_L = 100kΩ			±14.95			±14.95		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, Pin 1 = Open, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1150M MIN	LTC1150M TYP	LTC1150M MAX	LTC1150C MIN	LTC1150C TYP	LTC1150C MAX	UNITS
Slew Rate	R_L = 10kΩ, C_L = 50pF			3			3		V/µs
Gain Bandwidth Product				2.5			2.5		MHz
Supply Current	No Load No Load, Pin 1 = V^- No Load	 ●		0.8 0.2	1.5 2		0.8 0.2	1.5 2	mA
Internal Sampling Frequency				550			550		Hz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, Pin 1 = Open, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1150M MIN	LTC1150M TYP	LTC1150M MAX	LTC1150C MIN	LTC1150C TYP	LTC1150C MAX	UNITS
Input Offset Voltage	(Note 3)			±0.5	±10		±0.05	±10	µV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
Long Term Offset Voltage Drift				50			50		$\mu V/\sqrt{mo}$
Input Offset Current				±10	±60		±10	±60	pA
Input Bias Current				±5	±30		±5	±30	pA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz, TC2 R_S = 100Ω, 0.1Hz to 1Hz, TC2			2.0 0.7			2.0 0.7		μV_{P-P}
Input Noise Current	f = 10Hz (Note 4)			1.3			1.3		$fA/\sqrt{Hz}$
Common Mode Rejection Ratio	V_{CM} = 0V to 2.7V	●	106	130		106	130		dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	120	145		120	145		dB
Large-Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = 0.3V to 4.5V	●	115	180		115	180		dB
Maximum Output Voltage Swing	R_L = 10kΩ R_L = 100kΩ			0.15 to 4.85 0.02 to 4.97			0.15 to 4.85 0.02 to 4.97		V
Slew Rate	R_L = 10kΩ, C_L = 50pF			1.5			1.5		V/µs
Gain Bandwidth Product				1.8			1.8		MHz
Supply Current	No Load	 ●		0.4	1 1.5		0.4	1 1.5	mA
Internal Sampling Frequency				300			300		Hz

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1150.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high-speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

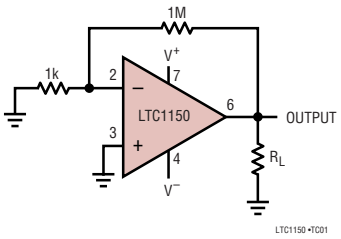
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{(2q \bullet I_b)}$$

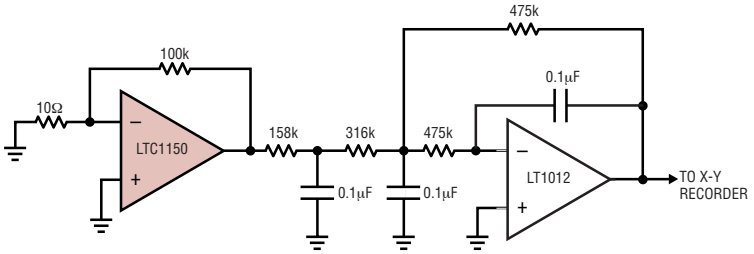
where $q = 1.6 \bullet 10^{-19}$ Coulomb.

TEST CIRCUITS

Offset Voltage Test Circuit



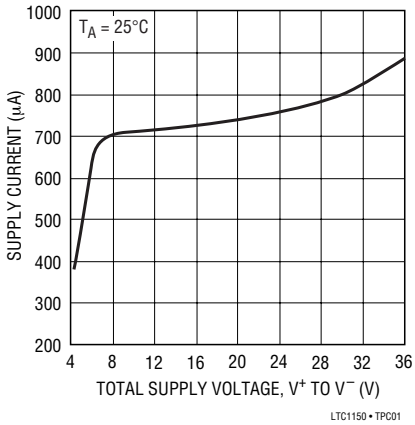
DC-10Hz Noise Test Circuit



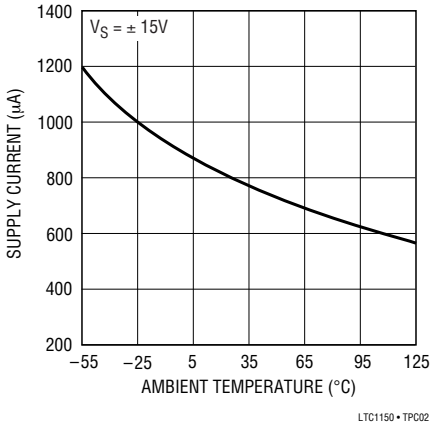
FOR 1Hz NOISE BW, INCREASE ALL THE CAPACITORS BY A FACTOR OF 10

TYPICAL PERFORMANCE CHARACTERISTICS

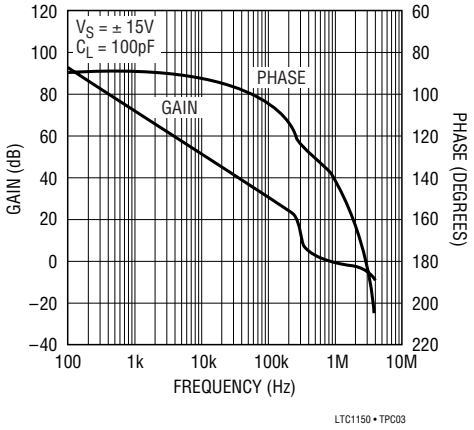
Supply Current vs Supply Voltage



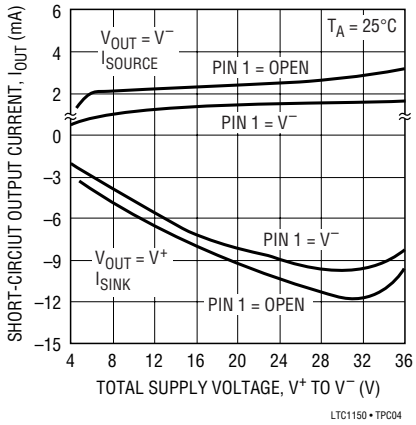
Supply Current vs Temperature



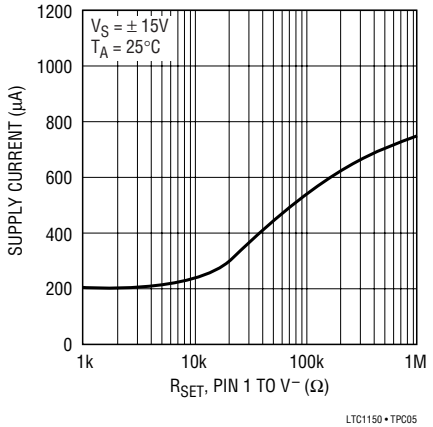
Gain/Phase vs Frequency



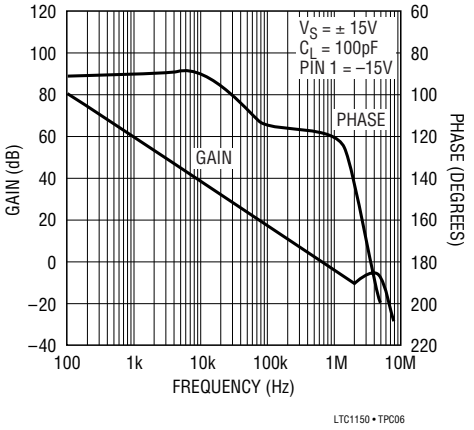
Output Short-Circuit Current vs Supply Voltage



Supply Current vs R_{SET}

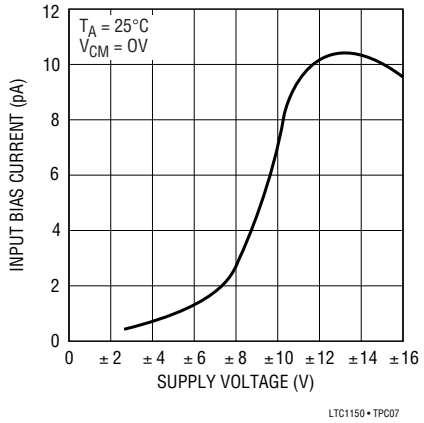


Gain/Phase vs Frequency



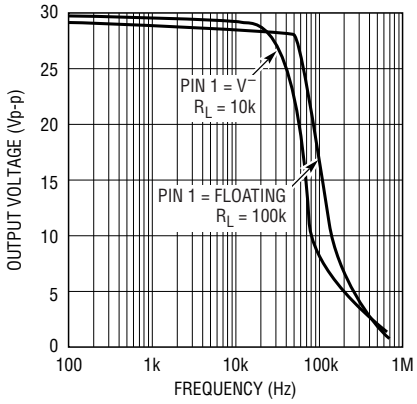
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Supply Voltage



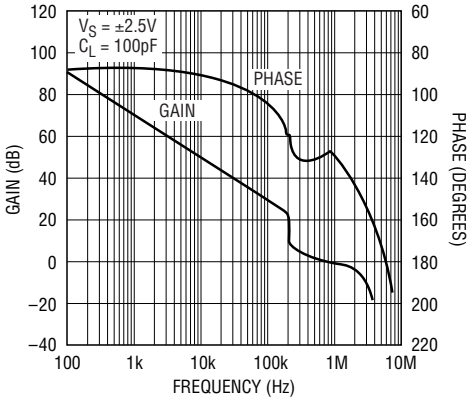
LTC1150 • TPC07

Undistorted Output Swing vs Frequency



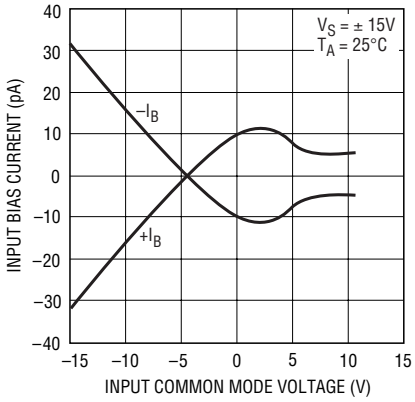
LTC1150 • TPC08

Gain/Phase vs Frequency



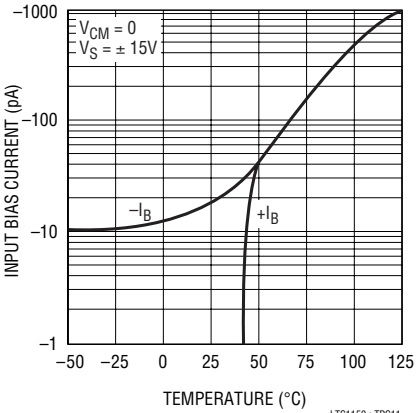
LTC1150 • TPC09

Input Bias Current vs Input Common Mode Voltage



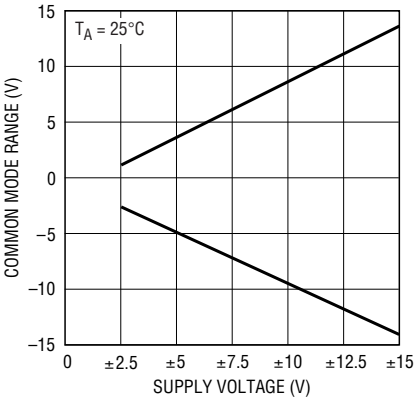
LTC1150 • TPC10

Input Bias Current vs Temperature



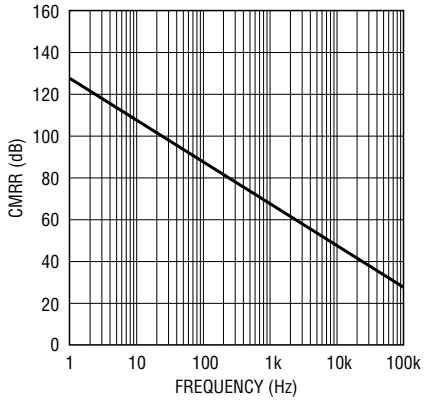
LTC1150 • TPC11

Common Mode Input Range vs Supply Voltage



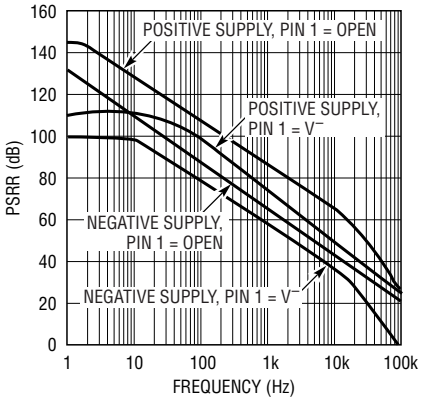
LTC1150 • TPC12

CMRR vs Frequency



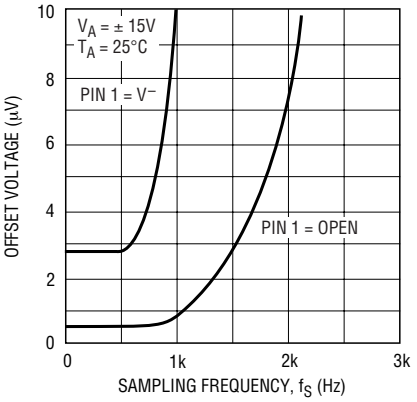
LTC1150 • TPC13

PSRR vs Frequency



LTC1150 • TPC14

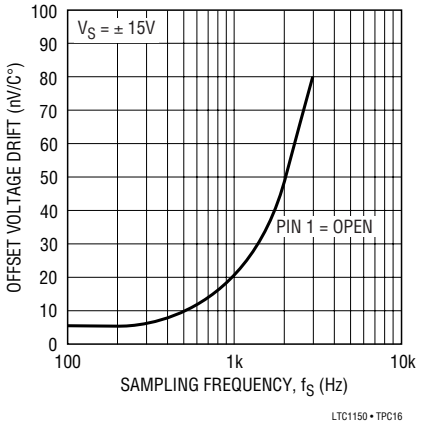
Offset Voltage vs Sampling Frequency



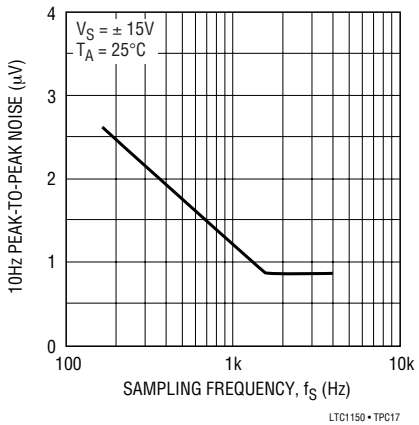
LTC1150 • TPC15

TYPICAL PERFORMANCE CHARACTERISTICS

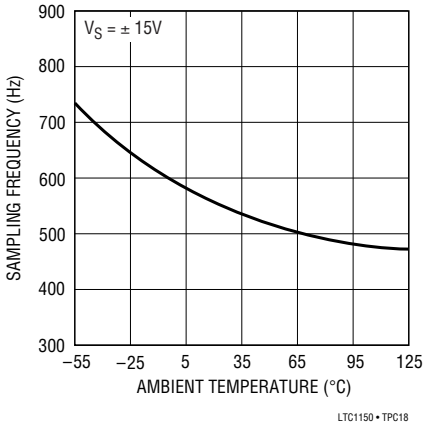
Offset Voltage Drift vs Sampling Frequency



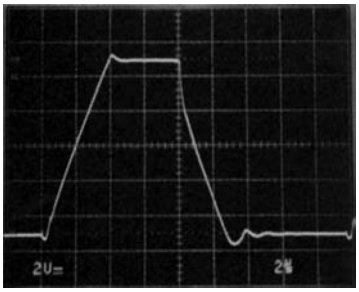
10Hz p-p Noise vs Sampling Frequency



Sampling Frequency vs Temperature

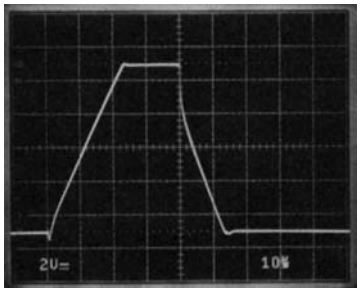


Large-Signal Transient Response



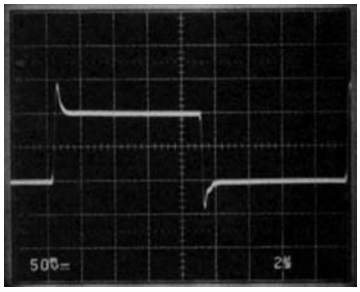
V_S = ±15V, A_V = 1, C_L = 100pF, R_L = 10kΩ

Large-Signal Transient Response, Pin 1 = V^-



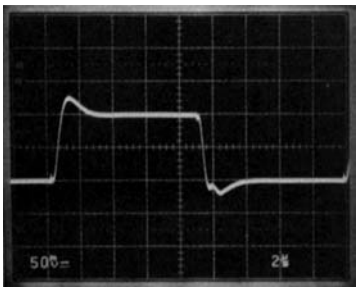
V_S = ±15V, A_V = 1, C_L = 100pF, PIN 1 = V^-

Small-Signal Transient Response



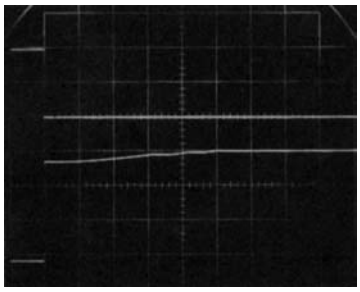
V_S = ±15V, A_V = 1, C_L = 100pF, R_L = 10kΩ

Small-Signal Transient Response, Pin 1 = V^-



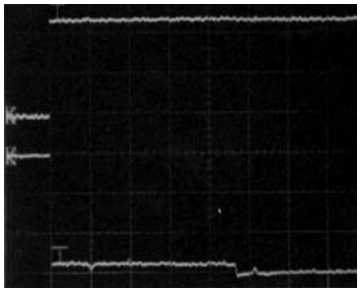
V_S = ±15V, A_V = 1, C_L = 100pF, R_L = 10kΩ, PIN 1 = V^-

Overload Recovery from Negative Saturation



V_S = ±15V, A_V = –100, 2ms/DIV

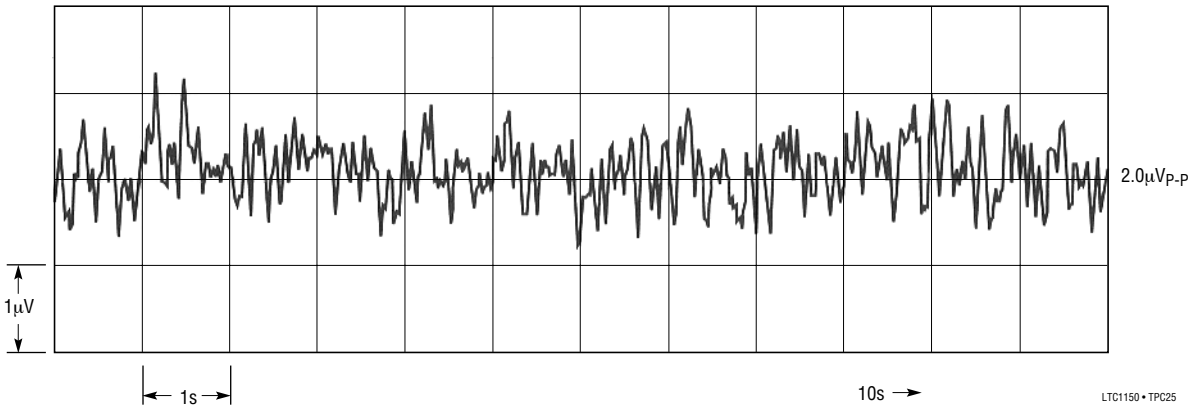
Overload Recovery from Positive Saturation



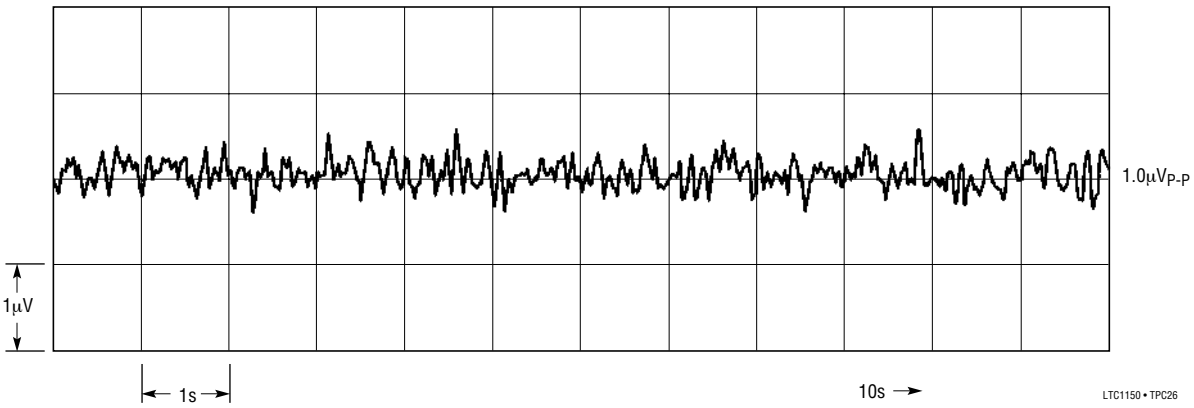
V_S = ±15V, A_V = –100, 2ms/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

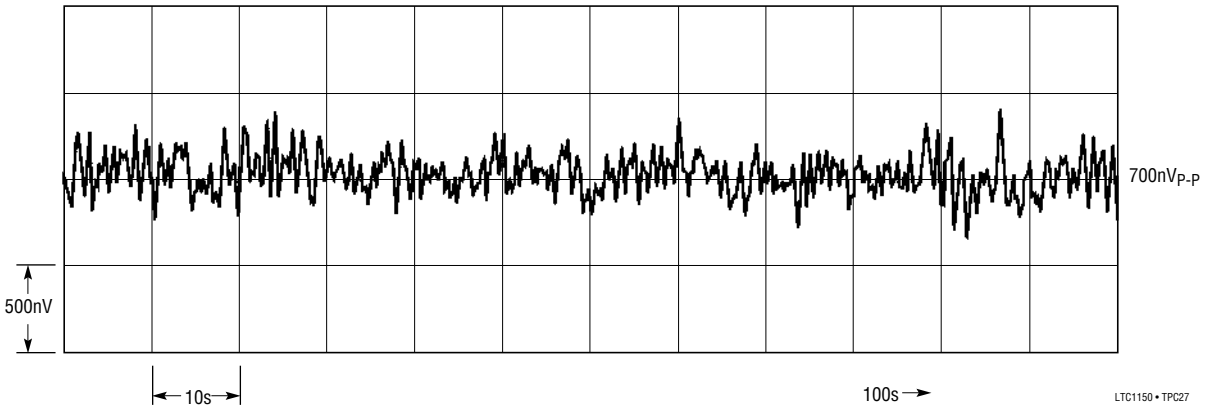
0.1Hz to 10Hz Noise, V = ±15V, T_A = 25°C, Internal Clock



0.1Hz to 10Hz Noise, V = ±15V, T_A = 25°C, f_S = 1800Hz

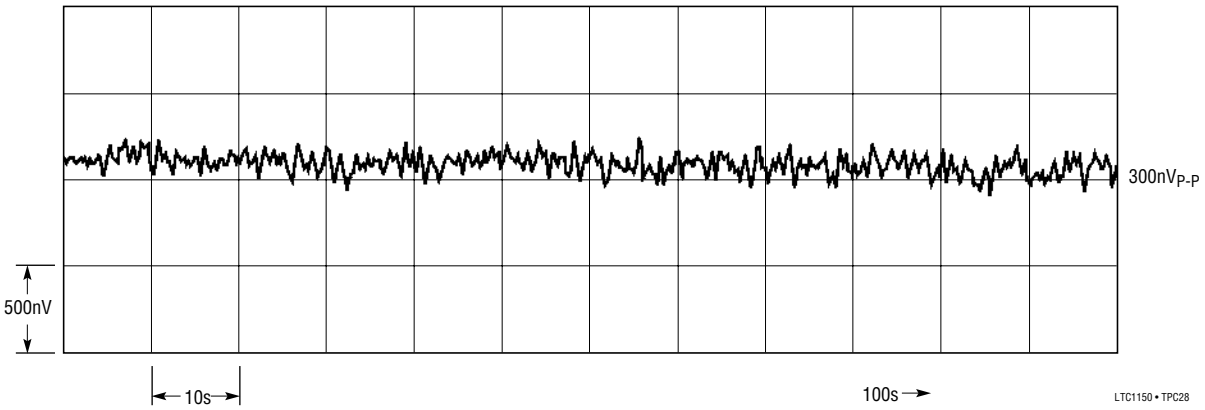


0.1Hz to 1Hz Noise, V = ±15V, T_A = 25°C, Internal Clock



TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 1Hz Noise, V = ±15V, T_A = 25°C, f_S = 1800Hz



PIN DESCRIPTIONS 8-Pin Packages

I_{SUPPLY} (Pin 1): Supply Current Programming. The supply current can be programmed through Pin 1. When Pin 1 is left open or tied to V^+, the supply current defaults to 800μA. Tying a resistor between Pin 1 and Pin 4, the negative supply pin, will reduce the supply current. The supply current, as a function of the resistor value, is shown in Typical Performance Characteristics.

–IN (Pin 2): Inverting Input.

+IN (Pin 3): Noninverting Input.

V^- (Pin 4): Negative Supply.

EXT CLOCK IN (Pin 5): Optional External Clock Input. The LTC1150 has an internal oscillator to control the circuit operation of the amplifier if Pin 5 is left open or biased at any DC voltage in the supply voltage range. When an external clock is desirable, it can be applied to Pin 5. The applied clock is AC-coupled to the internal circuitry to simplified interface requirements. The amplitude of the clock input signal needs to be greater than 2V and the voltage level has to be within the supply voltage range. Duty cycle is not critical. The internal chopping frequency is the external clock frequency divided by four. When frequency of the external clock falls below 100Hz (internal chopping at 25Hz), the internal oscillator takes over and the circuit chops at 550Hz.

OUT (Pin 6): Output.

V^+ (Pin 7): Positive Supply.

CLOCK OUT (Pin 8): Clock Output. The signal coming out of this pin is at the internal oscillator frequency of about 2.2kHz (four times the chopping frequency) and has voltage levels at $V_H = V_S$ and $V_L = V_S - 4.6$. If the circuit is driven by an external clock, Pin 8 is pulled up to V_S.

APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1150, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary–particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in noninverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1150's ultralow drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C—four times the maximum drift specification of the LTC1150. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C—700 times the maximum drift specification of the LTC1150.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches, and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 1 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

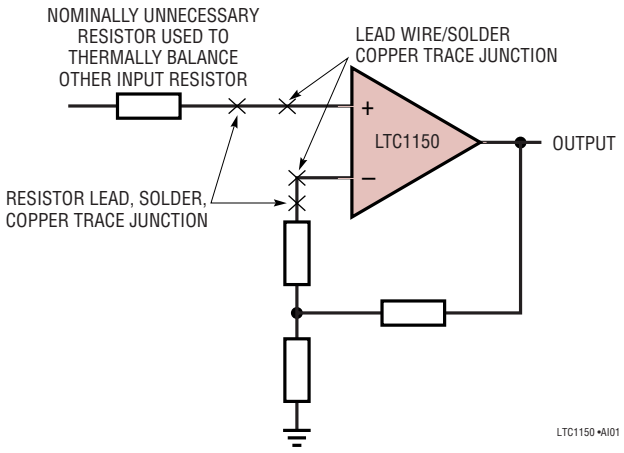


Figure 1. Extra Resistors Cancel Thermal EMF

When connectors, switches, relays and/or sockets are necessary, they should be selected for low thermal EMF activity. The same techniques of thermally-balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

APPLICATIONS INFORMATION

Table 1. Resistor Thermal EMF

RESISTOR TYPE	THERMAL EMF/°C GRADIENT
Tin Oxide	~mV/°C
Carbon Composition	~450μV/°C
Metal Film	~20μV/°C
WireWound Evenohm Manganin	 ~2μV/°C ~2μV/°C

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. It arises at the copper/kovar junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, it is outside the LTC1150's offset nulling loop and cannot be cancelled. Metal can H packages exhibit the worst warm-up drift. The input offset voltage specification of the LTC1150 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

ALIASING

Like all sampled data systems, the LTC1150 exhibits aliasing behavior at input frequencies near the sampling frequency. The LTC1150 includes a high-frequency correction loop which minimizes this effect; as a result, aliasing is not a problem for most applications.

For a complete discussion of the correction circuitry and aliasing behavior, please refer to the LTC1051/53 data sheet.

SYNCHRONIZATION OF MULTIPLE LTC1150'S

When synchronization of several LTC1150's is required, one of the LTC1150's can be used to provide the "master" clock to control over 100 "slave" LTC1150's. The master clock, coming from Pin 8 of the master LTC1150, can directly drive Pin 5 of the slaves. Note that Pin 8 of the slave LTC1150's will be pulled up to V_S.

If all the LTC1150's are to be synchronized with an external clock, then the external clock should drive Pin 5 of all the LTC1150's.

LEVEL SHIFTING THE CLOCK

Level shifting is needed if the clock output of the LTC1150 in ±15V operation must interface to regular 5V logic circuits. Figures 2 and 3 show some typical level shifting circuits.

When operated from single 5V or ±5V supplies, the LTC1150 clock output at Pin 8 can interface to TTL or CMOS inputs directly.

LOW SUPPLY OPERATION

The minimum supply for proper operation of the LTC1150 is typically below 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V) to ensure proper operation down to the minimum TTL specified voltage of 4.75V.

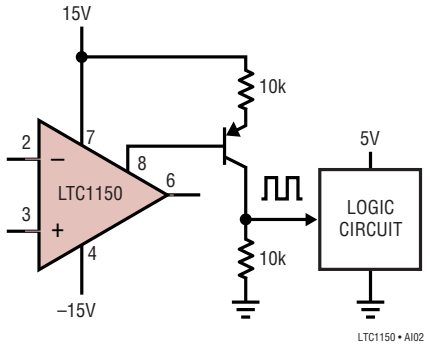


Figure 2. Output Level Shift (Option 1)

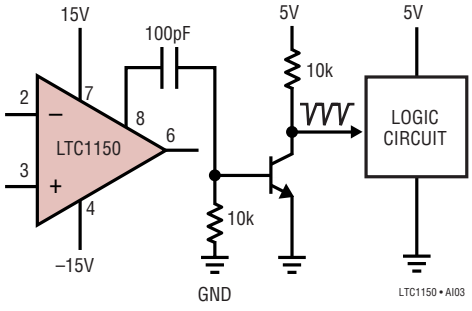
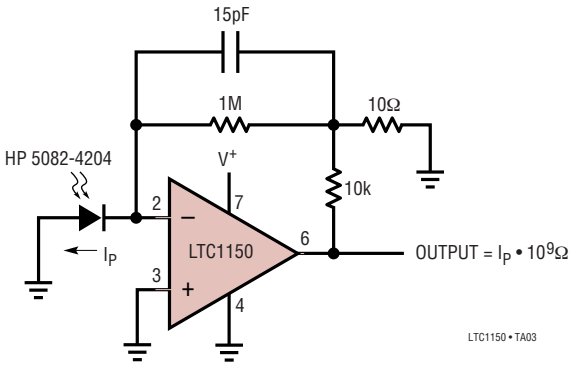


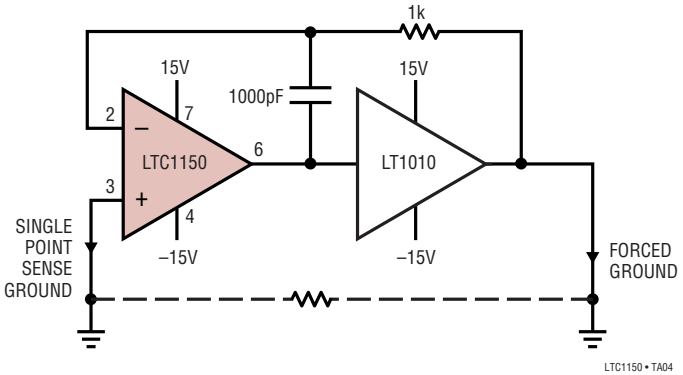
Figure 3. Output Level Shift (Option 2)

TYPICAL APPLICATIONS

Low Level Photodetector



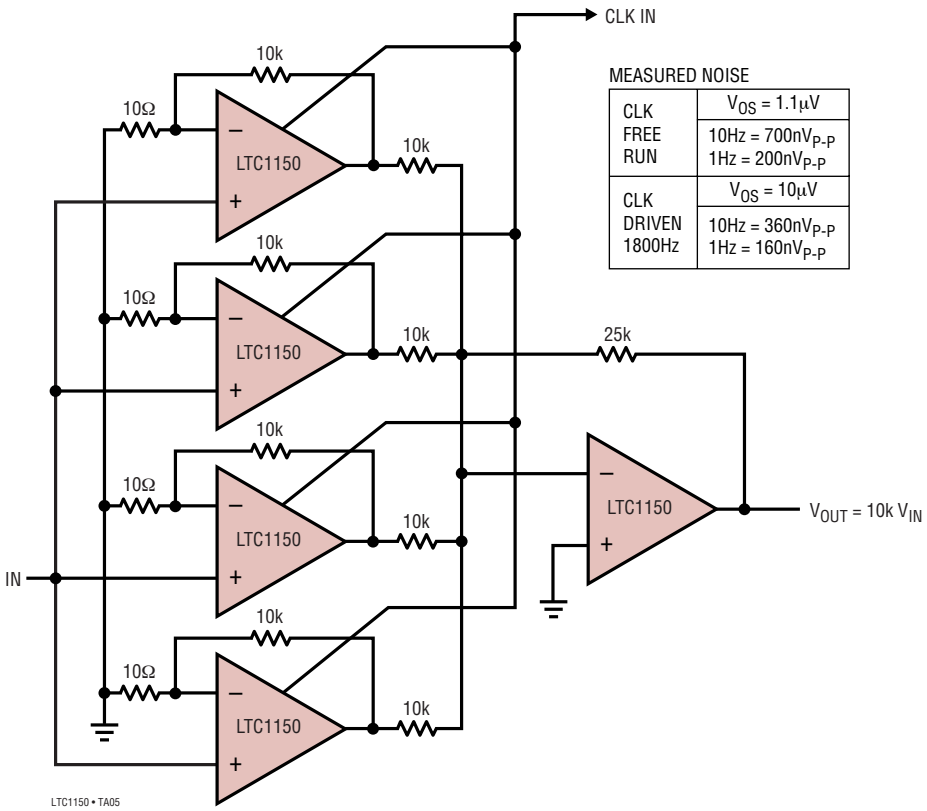
Ground Force Reference



APPLICATION: TO FORCE TWO GROUND POINTS IN A SYSTEM WITHIN 5μV

TYPICAL APPLICATIONS

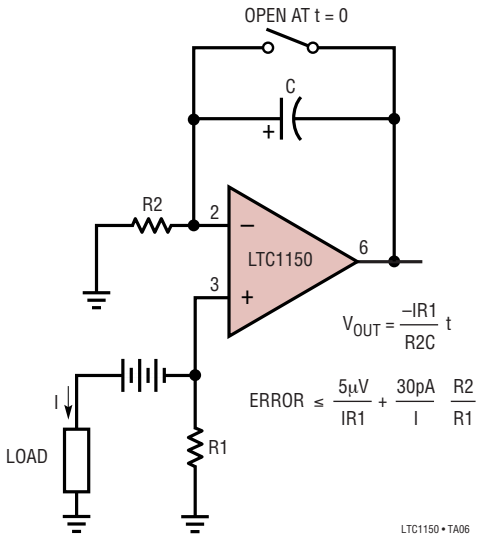
Paralleling to Improve Noise



MEASURED NOISE

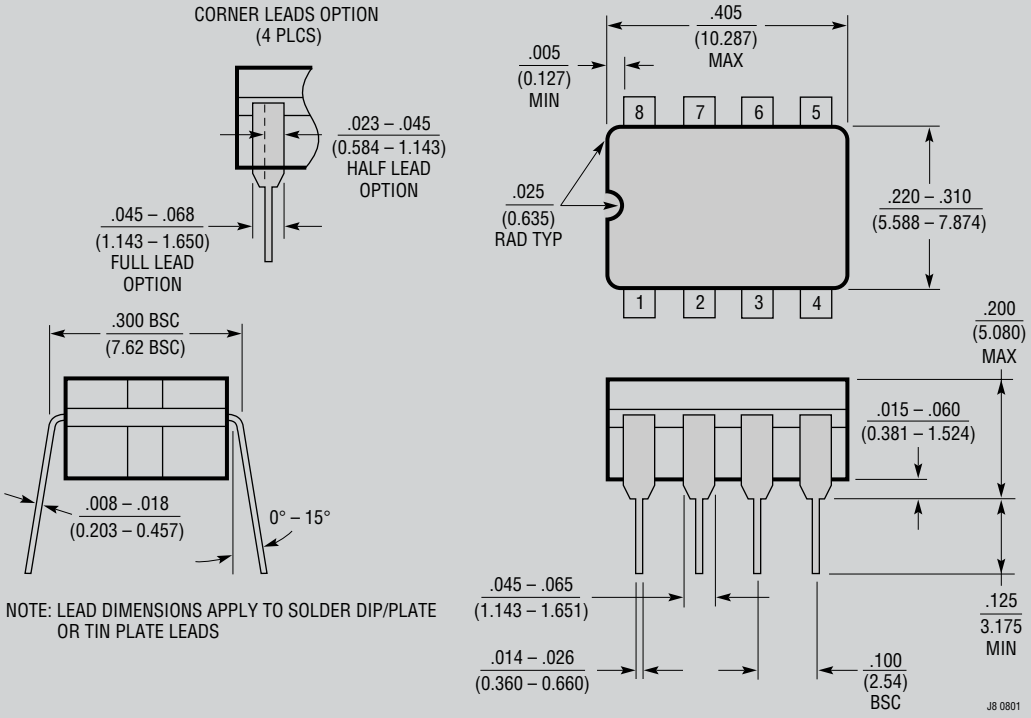
CLK FREE RUN	V_{OS} = 1.1μV
	10Hz = 700nV_{P-P}
	1Hz = 200nV_{P-P}
CLK DRIVEN 1800Hz	V_{OS} = 10μV
	10Hz = 360nV_{P-P}
	1Hz = 160nV_{P-P}

Battery Discharge Monitor



PACKAGE DESCRIPTION

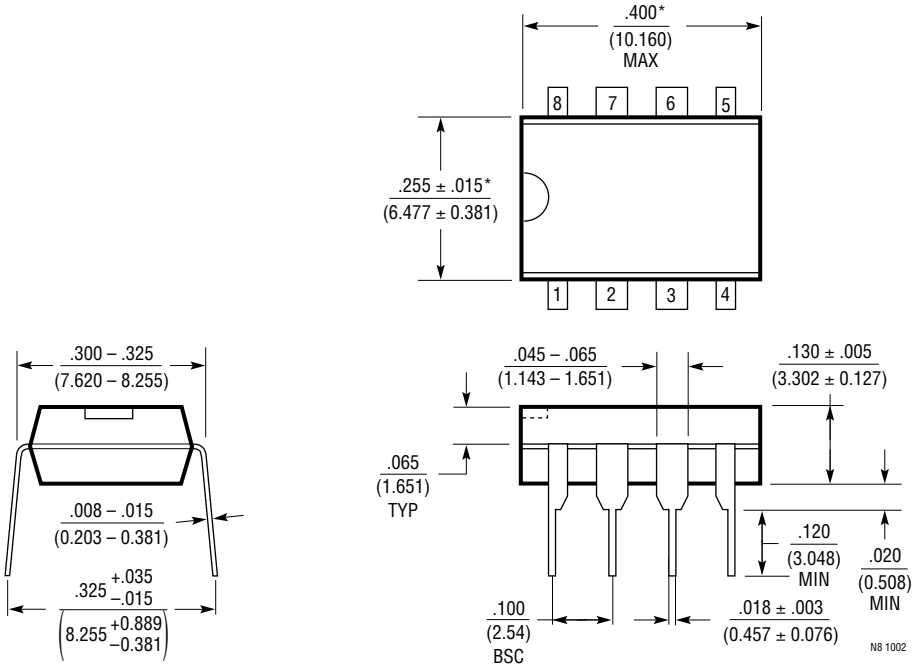
J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

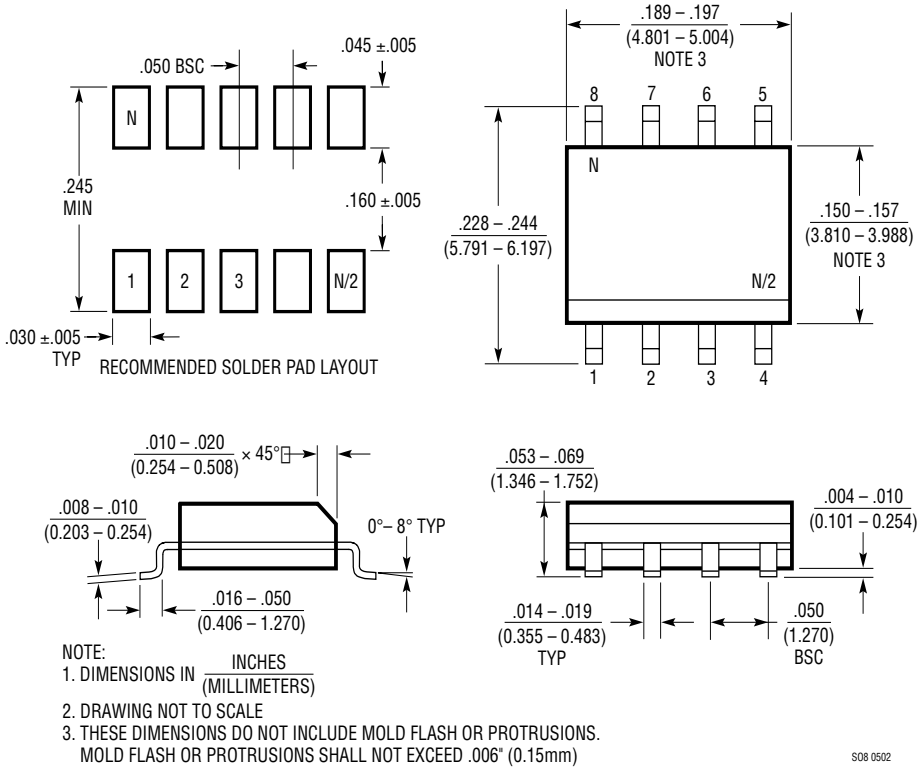


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

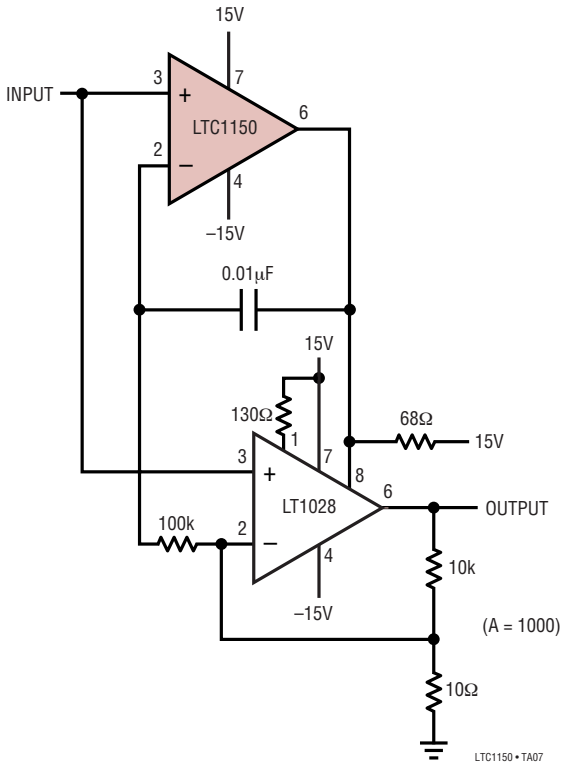


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0502

TYPICAL APPLICATION

DC Stabilized, Low Noise Amplifier



Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LW/TP 1202 1K REV B • PRINTED IN USA